AS3980

UHF RFID Single Chip Reader EPC Class1 Gen2

General Description

The AS3980 is an UHF RFID reader IC enabling battery-powered, small form-factor handheld and embedded UHF reader systems for a single tag environment of EPC Class1 Gen2 compliant UHF RFID tags. The device directly supports ISO 18000-6C/ EPC Class1 Gen2 transponders in a single-tag environment. The AS3980 operates at very low power, which means that this advanced RFID reader IC is suitable for use in portable and battery-powered equipment such as mobile phones. AS3980 requires only an external simple 8-bit µC to create a complete RFID reader system. AS3980 is highly integrated and implements the RFID functions on chip thus eliminating a need for a complex RFID co-processor. Packaged in a 7 x 7 mm QFN outline, the IC benefits from fabrication process technology unique to **ams** to deliver very high sensitivity and providing high immunity to the effects of antenna reflections and self-jamming. This is critical in mobile and embedded applications, in which antenna design is often compromised by cost or size constraints. High sensitivity enables end-product designs to achieve their required read range while using a simpler and cheaper antenna, thus reducing system bill-of-materials cost.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3980, UHF RFID Single Chip Reader EPC Class1 Gen2 are listed below:

Figure 1:
Added Value of Using AS3980

Benefit	Feature

Optimized for battery operation	• Supply voltage range 3.0V to 3.6V
	  • Limited operation possible down to 2.7V
	  • Peripheral I/O supply range: 1.65V to 5.5V

ISO 18000-6C implemented in HW.	• Basic protocol support for ISO 18000-6C (EPC Class1 Gen2) • Reception mode M8 on 40kHz link frequency
Low coding effort and MCU requirements	
High PSRR	• Integrated supply regulators
Flexible modulation method	• ASK or PR-ASK modulation
Small package footprint – saving PCB area	• 48-pin QFN (7x7x0.9 mm) package

Benefit	Feature
Avoidance of communication holes	• Automatic I/Q selection
Tag movement detection support	• Phase bit for tag tracking with 8-bit linear RSSI
Wide temperature range	• -40ºC to 85ºC

Applications

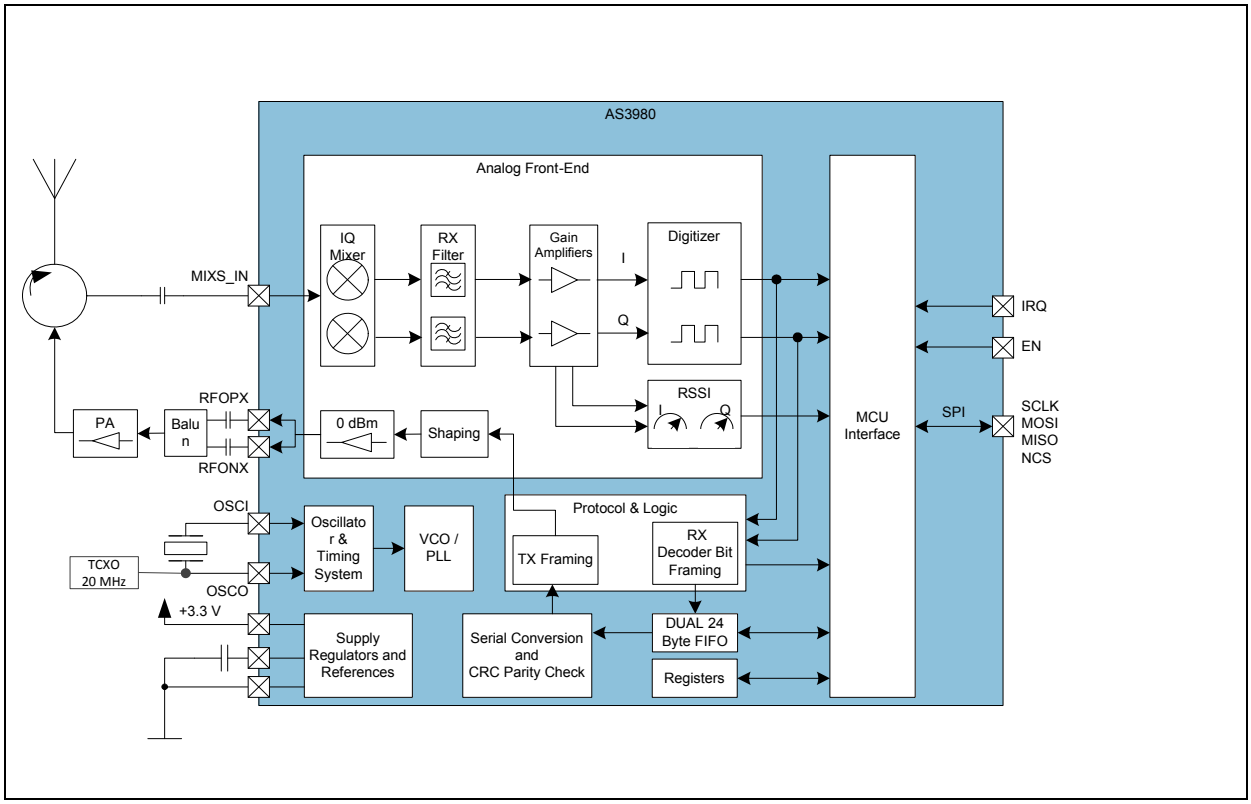
The AS3980 device is well suited for:

- Embedded consumer/industrial applications with cost constraints such as beverage dispensing.
- Hand-Held readers.
- Mobile UHF RFID readers.
- Battery-Powered stationary readers.
- FMCG and brand protection
- Product authentication

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
AS3980 Block Diagram



Pin Assignment

The AS3980 pin assignments are described below.

Figure 3:
Pin Diagram

AS3980 Pin Assignment: This figure shows the pin assignment and location viewed from top.

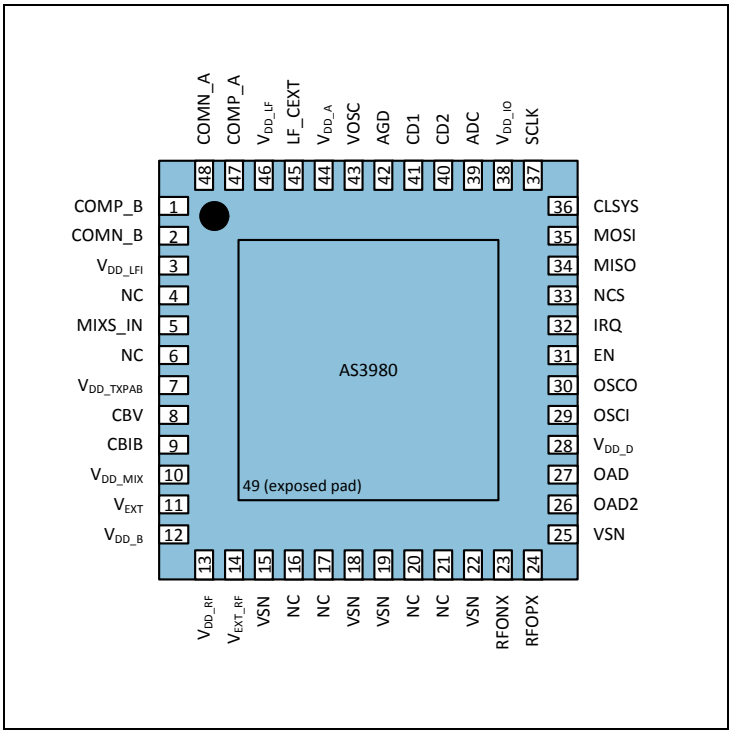


Figure 4:
Pin Description

Pin Number 48-Pin QFN	Pin Name	Pin Type	Description
1	COMP_B	Analog I/O	Internal node, connect de-coupling capacitor to V_{DD_LFI}
2	COMN_B	Analog I/O	Internal node, connect de-coupling capacitor to V_{DD_LFI}
3	V_{DD_LFI}	Supply pad	Positive supply for LF input stage, connect to V_{DD_MIX}
4	NC		Not connected
5	MIXS_IN	Analog input	Single ended mixer input
6	NC		Not connected
7	V_{DD_TXPAB}	Supply pad	Bias positive supply. Connect to V_{DD_MIX}
8	CBV	Analog I/O	Internal node, connect de-coupling capacitor to V_{DD_MIX}
9	CBIB	Analog I/O	Internal node, connect de-coupling capacitor to ground
10	V_{DD_MIX}	Analog I/O	Mixer positive supply, internally regulated

Pin Number 48-Pin QFN	Pin Name	Pin Type	Description
11	V_{EXT}	Supply pad	Main positive supply input, input to regulators
12	V_{DD_B}	Analog I/O	Buffer positive supply, internally regulated
13	V_{DD_RF}	Analog I/O	RF positive supply, internally regulated
14	V_{EXT_RF}	Supply pad	RF positive supply regulator input
15	VSN	Supply pad	Negative supply
16	NC		Not connected
17	NC		Not connected
18	VSN	Supply pad	Negative supply
19	VSN	Supply pad	Negative supply
20	NC		Not connected
21	NC		Not connected
22	VSN	Supply pad	Negative supply
23	RFONX	Analog output	Low power linear negative RF output (~0dBm)
24	RFOPX	Analog output	Low power linear positive RF output (~0dBm)
25	VSN	Supply pad	Negative supply
26	OAD2	Analog I/O	Analog or digital received signal output
27	OAD	Analog I/O	Analog or digital received signal output
28	V_{DD_D}	Analog I/O	Positive supply for logic, internally regulated
29	OSCI	Analog input	Crystal oscillator input or short to ground in case external TCXO is used
30	OSCO	Analog I/O	Crystal oscillator output or external 20MHz clock input
31	EN	Digital input	Enable input
32	IRQ	Digital output	Interrupt request output
33	NCS	Digital input	Serial Peripheral Interface Enable (active low)
34	MISO	Digital output / tri-state	Serial Peripheral Interface DATA output
35	MOSI	Digital input	Serial Peripheral Interface DATA input
36	CLSYS	Digital output	Clock Output for MCU
37	SCLK	Digital input	Serial Peripheral Interface Clock

Pin Number 48-Pin QFN	Pin Name	Pin Type	Description
38	V_{DD_IO}	Supply pad	Positive supply for peripheral communication, connect to host positive supply
39	ADC	Analog input	ADC input for external power detector support
40	CD2	Analog I/O	Internal node de-coupling capacitor
41	CD1	Analog I/O	Internal node de-coupling capacitor
42	AGD	Analog I/O	Analog reference voltage
43	VOSC	Analog I/O	Internal node de-coupling capacitor
44	V_{DD_A}	Analog I/O	Analog part positive supply, internally regulated
45	LF_CEXT	Analog output	PLL Loop filter
46	V_{DD_LF}	Analog I/O	Positive supply for LF processing, internally regulated
47	COMP_A	Analog I/O	Internal node, connect de-coupling capacitor to V_{DD_LFI}
48	COMN_A	Analog I/O	Internal node, connect de-coupling capacitor to V_{DD_LFI}
49	Exposed Pad	Supply pad	Exposed pad of the package

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD_IO}	Supply voltage V_{DD_IO}	-0.3	6.0	V	
V_{EXT}	Supply voltage V_{EXT}	-0.3	4	V	
V_{EXT_RF}	Supply voltage V_{EXT_RF}	-0.3	4.5	V	
V_{INH}	Input pin voltage host interface	-0.3	V_{DD_IO} + 0.5	V	Valid for inputs EN, IRQ, MOSI, SCLK, NCS
V_{INO}	Input pin voltage, other pins	-0.3	V_{EXT} + 0.5	V	
I_scr	Input current (latch-up immunity)	-100	100	mA	Norm: JEDEC 78, AGD excluded from Latch-up immunity test for EN is high. AGD is a reference voltage pin and must be kept at the reference
Electrostatic Discharge					
ESD_{HBM}	Electrostatic discharge for the RF pins 5, 23 and 24	±1		kV	Norm: JESD22-A114E
	Electrostatic discharge for other pins	±2		kV	
Continuous Power Dissipation					
P_T	Total power dissipation (all supplies and outputs)		1.6	W	

Symbol	Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions					
T_J	Maximum operating virtual junction temperature		120	°C	
T_{strg}	Storage temperature	-55	125	°C	
T_{body}	Package Body Temperature		260	°C	Norm: IPC/JEDEC J-STD-020. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”
RH_{NC}	Relative Humidity non-condensing	5	85	%	
MSL	Moisture Sensitivity Level	3			Represents a max. floor life time of 168h

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

V_{EXT} = 3.3 V, V_{EXT_RF} = 3.3 V, V_{DD_IO} = 3.3 V, T_A = 25 °C unless otherwise noted.

Figure 6:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{EXT}	Supply current without VDD_RF current	V_{EXT} consumption	65 (1)	75		mA
I_{STBY}	Supply current in standby mode			3		mA
I_{PD}	Supply current in power-down mode	All system disabled including supply voltage regulators		1	10	µA
V_{AGD}	AGD voltage		1.45	1.55	1.65	V
V_{POR}	Power on reset voltage (POR)		1	1.8	2.0	V
V_{RD}	Regulator drop	see note (2)		300		mV
P_{PSSR}	Rejection of external supply noise on the supply regulator	see note (3)		26		dB
P_{RF}	RF output power	V_{DD_B} =3V		0		dBm
R_{RFIN}	Single ended mixer input impedance			50		Ω
V_{SENS_NOM}	Input sensitivity	Nominal mixer setting, PER=0.1%		-67		dBm
V_{SENS_GAIN}	Input sensitivity	Increased mixer gain, PER=0.1%		-77		dBm
V_{SENS_LBT}	LBT sensitivity	Maximum LBT sensitivity		-90		dBm
IP3	Third order intercept point	Nominal mixer setting (4) VEXT = 3V		17		dBm
$1dB_{CP}$	Input 1dB compression point	Nominal mixer setting (4) VEXT = 3V		7		dBm
T_{REC}	Recovery time after modulation	Maximum LF selected		18		µs

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS Input (valid for all CMOS inputs)						
V_{IH}	High level input voltage	see note (5)	0.8 * V_{DD_IO}			V
V_{IL}	Low level input voltage	see note (6)			0.2 * V_{DD_IO}	V
I_{LEAK}	Input leakage current				1	µA
CMOS Output (valid for all CMOS outputs) **Note:** On all outputs, it is recommended to use loads with the smallest required drive capability in order to prevent current/spikes problems.						
f_{SCLK}	SCLK frequency	**hs_output** = 1 (7), $V_{DD_IO} \geq 3V$, $C_{LOAD} = 50pF$			5	MHz
		hs_output = 1, $V_{DD_IO} \geq 1.65V$, $C_{LOAD} = 50pF$			3	MHz
		hs_output = 0, $V_{DD_IO} \geq 3V$, $C_{LOAD} = 50pF$			2	MHz
R_{NMOS}	Output NMOS resistance on digital pins	**hs_output** = 1		120		Ω
R_{PMOS}	Output PMOS resistance on digital pins	**hs_output** = 1, $V_{DD_IO} > 3V$		150		Ω
		hs_output = 1, $V_{DD_IO} > 1.65V$		300		Ω

Note(s) and/or Footnote(s):

1. Using **ic_bia_m<1:0>** option bits, the consumption can be decreased up to 9%. The drawback of decreased power consumption can be higher noise, lower output power, and declining sensitivity.
2. After execution of direct command: Automatic Power Supply Level Setting ($A2_h$).
3. The difference between the external supply and the regulated voltage is higher than 300mV.
4. Register settings for nominal mixer settings: $0A:01_h$, $0D:84_h$, $22:13_h$.
5. At supply voltage ≤1.8V, the minimum VIH is defined as $0.9*V_{DD_IO}$.
6. At supply voltage ≤1.8V, the maximum VIL is defined as $0.1*V_{DD_IO}$.
7. Option bit 7 of Miscellaneous Register 1.

Typical Operating Characteristics

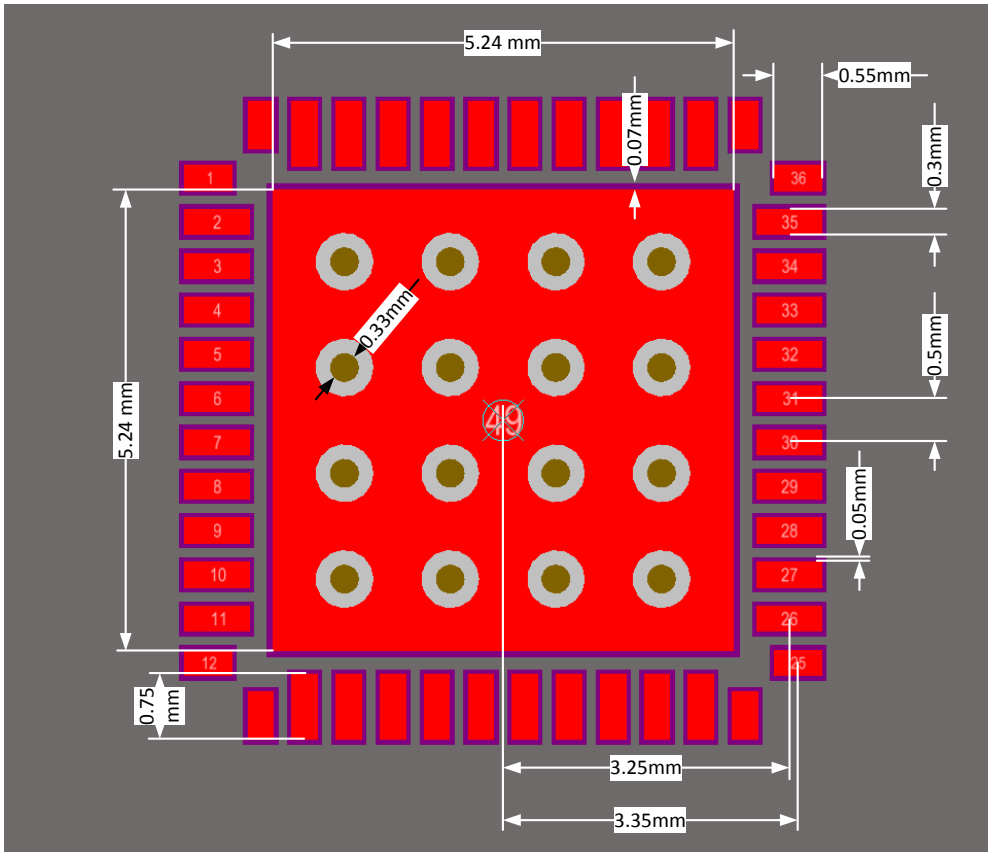
All in this specification defined tolerances for external components need to be assured over the whole operation condition range and also over lifetime.

Figure 7:
Typical Operating Characteristics

Symbol	Parameter	Min	Max	Units	Comments
V_{DD_IO}	Positive supply voltage V_{DD_IO}	1.65	5.5	V	
V_{EXT}	Positive supply voltage V_{EXT}	2.7	3.6	V	For optimal power supply rejection and performance a supply voltage of at least 3.3 V is required. A supply voltage above 3.0V allows operation with reduced power supply rejection. Operation down to 2.7V is possible with reduced performance.
V_{EXT_RF}	Positive supply voltage V_{EXTRF}	2.7	4.3	V	
V_{SS}	Negative supply voltage	0	0	V	Valid for all VSS and VSN pins
T_{AMB}	Ambient temperature	-40	85	°C	

PCB Pad Layout

Figure 8:
Recommended PCB Pad Layout



AS3980 PCB Pad Layout : This figure shows the recommended PCB land pattern of the AS3980 device.

Soldering Information

Stencil Design & Solder Paste Application

1. Stainless steel stencils are recommended for solder paste application.
2. A stencil thickness of 0.125 – 0.150 mm (5 – 6 mils) is recommended for screening.
3. For the PCB thermal pad, solder paste should be printed on the PCB by designing a stencil with an array of smaller openings that sum to 50% of the QFN thermal pad area as shown in Figure 9.
4. The aperture opening for the signal pads should be between 50-80% of the QFN pad area as shown in Figure 10.
5. Optionally, for better solder paste release, the aperture walls should be trapezoidal and the corners rounded.
6. The fine pitch of the IC leads requires accurate alignment of the stencil and the printed circuit board. The stencil and printed circuit assembly should be aligned to within + 1 mil prior to application of the solder paste.
7. No-clean flux is recommended since flux from underneath the thermal pad will be difficult to clean if water-soluble flux is used.

Figure 9:
Solder Paste Application on Paddle

Solder Paste Paddle Pattern: Solder paste should be applied through an array of squares (or circles) which totals 50 % of the total area of the paddle.

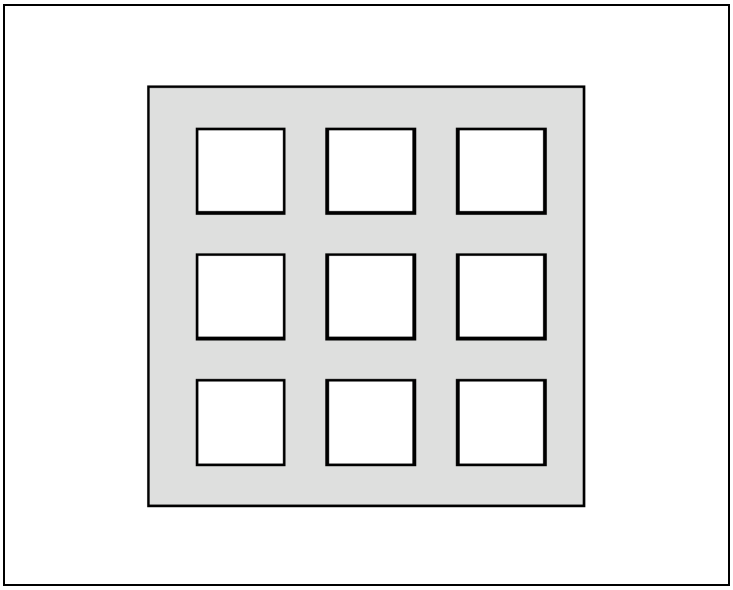
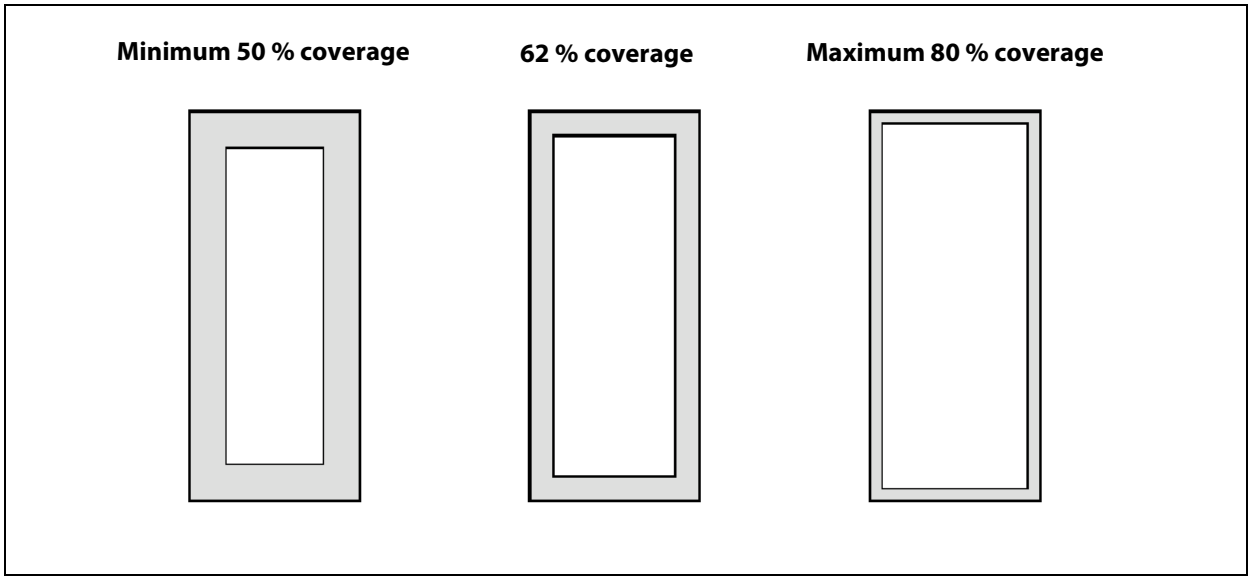


Figure 10:
Solder Paste Application on Pads



Solder Paste on Pads: The aperture opening for the signal pads should be between 50-80% of the QFN pad area.

Soldering Options & Package Placement

1. Hand soldering of these devices is not recommended even for prototypes.
2. Infrared or Convection mass reflow soldering is the preferred method of QFN attachment.
3. Manual placement and/or manual repositioning of QFN packages is not recommended.

Solder Reflow Profile

The PCB assembly should be instrumented and the reflow oven's process parameters established to ensure the solder paste manufacturer's reflow profile specification is met during the assembly process. See Figure 12.

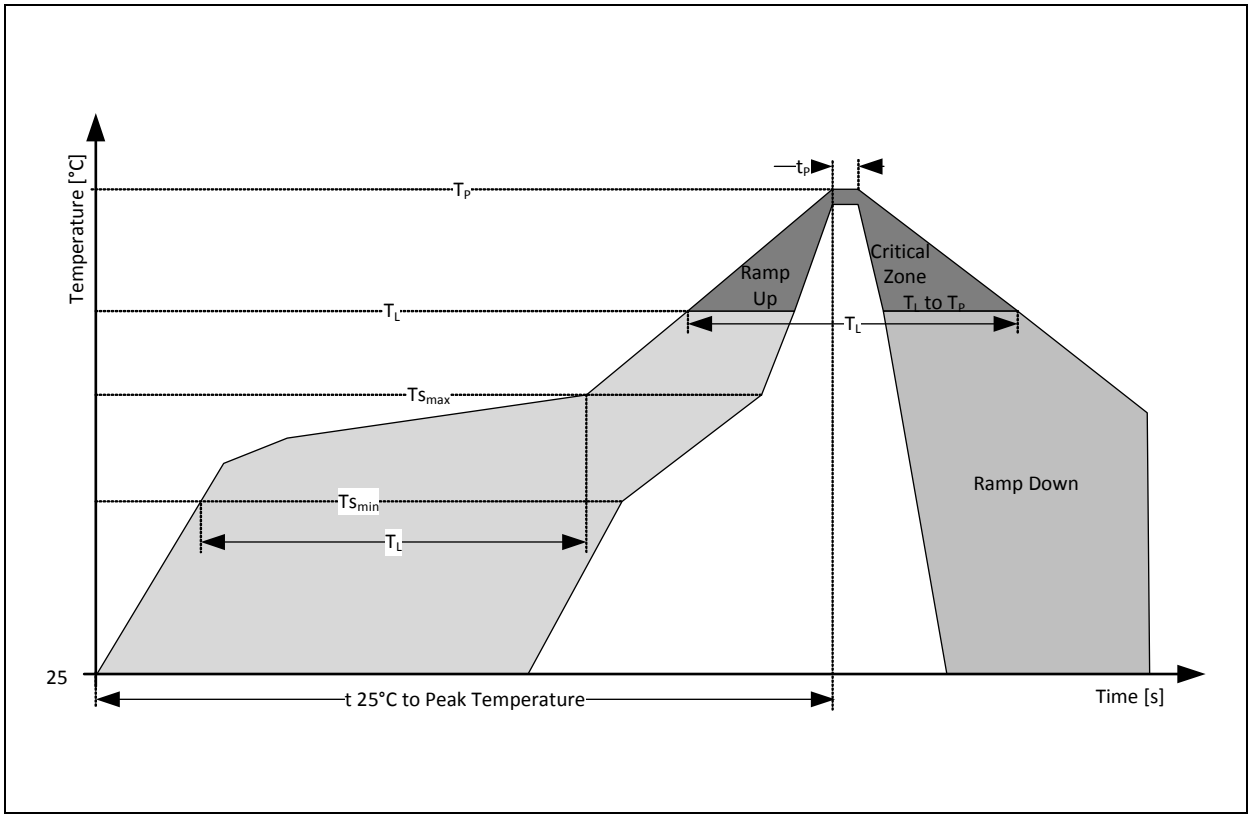
The maximum PCB temperature recommended by the supplier must not be exceeded.

Figure 11:
Solder Reflow Profile

Profile Feature	Lead-free Assembly
Average ramp-up rate (Ts_{max} to T_P)	3 °C/second max.
Preheat • Temperature Min (Ts_{min}) • Temperature Max (Ts_{max}) • Time (t_L)	150 °C 200 °C 60 – 120 seconds
Time maintained above: • Temperature (T_L) • Time (t_L)	217 °C 60 – 150 seconds
Peak/classification temperature (T_P)	260 °C
Time within 5 °C of actual peak temperature (T_P)	30 seconds
Ramp-down rate	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

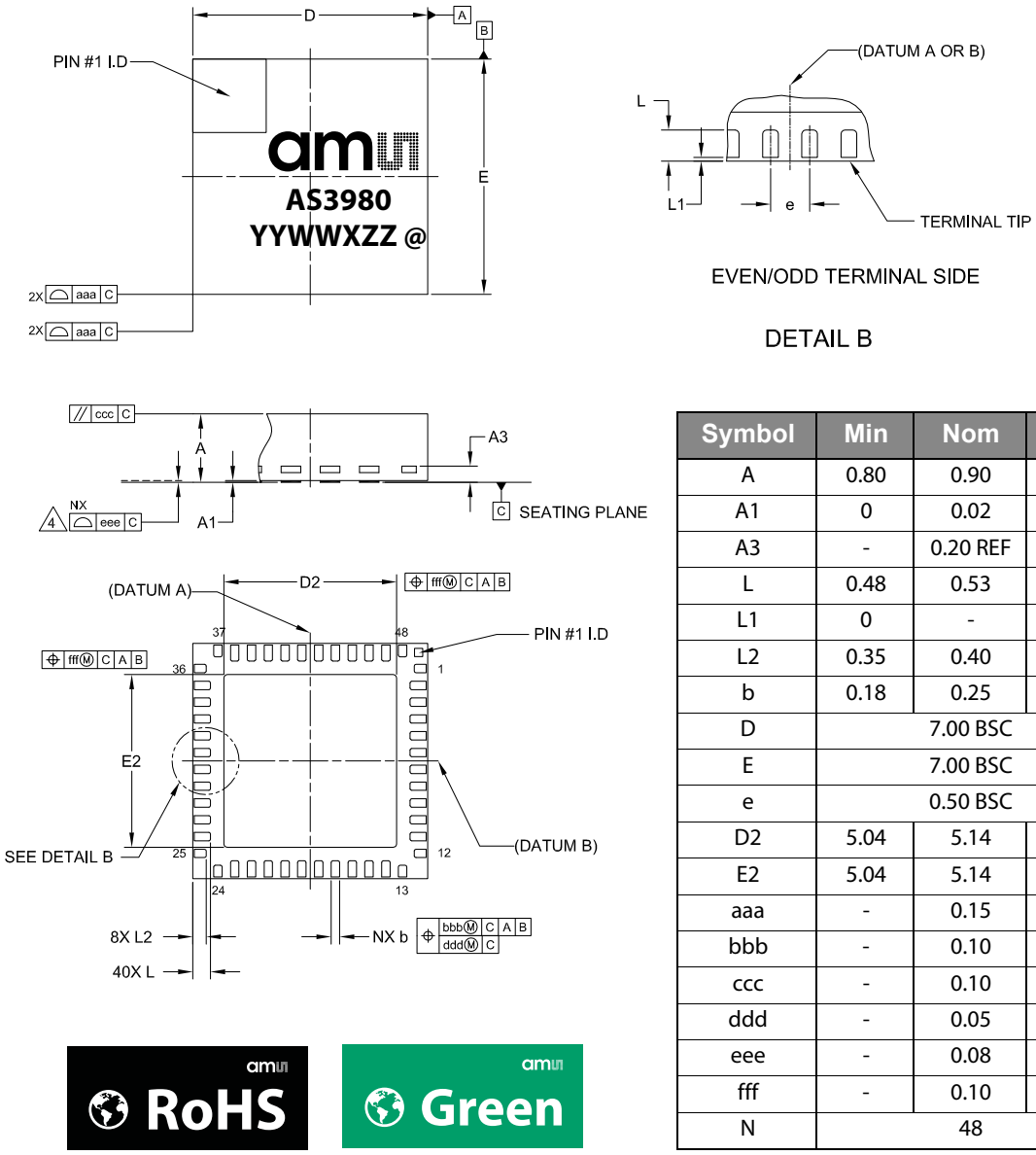
JEDEC standard Lead-free reflow profile: According to J-STD-020D.

Figure 12:
Recommended Reflow Soldering Profile



Package Drawings & Markings

Figure 13:
Package Drawings



Symbol	Min	Nom	Max
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	-	0.20 REF	-
L	0.48	0.53	0.58
L1	0	-	0.15
L2	0.35	0.40	0.45
b	0.18	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
D2	5.04	5.14	5.24
E2	5.04	5.14	5.24
aaa	-	0.15	-
bbb	-	0.10	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		48	

Note(s) and/or Footnote(s):

1. Dimensioning and tolerances conform to *ASME Y14.5M-1994*.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.15mm is acceptable.
4. Co-planarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.
6. N is the total number of terminals.
7. This drawing is subject to change without notice.

Figure 14:
Packaging Code YYWWXZZ@

YY	WW	X	ZZ	@
Year	Working week assembly / packaging	Plant identifier	Free choice / traceability code	Sublot Identifier

Packaging Code YYWWXZZ: This figure explains the laser marked date code on the package.

Ordering & Contact Information

Figure 15:
Ordering Information

Ordering Code	Package	Marking	Delivery Form	Delivery Quantity
AS3980-BQFM	48-pin QFN (7x7x0.9 mm)	AS3980	Tape & Reel	50
AS3980-BQFT				500

Ordering Information: This figure shows ordering information for the AS3980 device.

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Revision Information

The initial version of short datasheet was derived from version 2-01 of full datasheet.

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